High Efficient Comparator Based CMOS Active Rectifier for Biomedical Implants

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Abstract. Most of the biomedical implants uses wireless power transfer techniques. The main limitations of these technique is in their circuitry interface and consistent provision of a stable and reliable power supply. By adopting the high speed comparator in proposed rectifier solved the turn on and off delay of power transistor problem of conventional rectifier and shows high power conversion efficiency. A switched-offset biasing is used to compensate for delays inherent in active diodes and to remove both reverse current and multiple pulsing. The comparator’s bias voltage is generated using a peaking current source that is inversely proportional to the DC output voltage, allowing better control of the comparator over a wide range of AC input voltages.

Keywords: Wireless power transfer, Active rectifier, Switched offset

1 Introduction

Most of the biomedical devices are powered wirelessly. Medical researchers are started focusing on implanted devices such as cochlear, retinal, and even brain implants to restore and/or monitor biological functions. The continued growth in this field will result in a diverse market for wirelessly powered on-chip solutions. Power signal’s frequency is one of the key factors in wireless power transfer. A frequency of 13.56 MHz is typically used in wirelessly powered biomedical devices because of the frequency’s ability to couple with near-field receivers and its power attenuation characteristics through human tissue. Once the AC signal is on chip, it must be rectified to a DC voltage.

Fig.1. Block diagram of a typical wireless power transfer system.

The simplest way to rectify an AC signal is by using a passive rectifier, implemented as a diode bridge. However, the forward voltage drop of each diode severely reduces the voltage conversion ratio. Thus, in order to maintain a large enough DC output voltage using a passive rectifier, a large AC input voltage is required in order to overcome the overdrive voltage drops. This problem can be overcome by using an active rectifier, where the diode bridge’s top diodes are replaced with cross coupled PMOS transistors, and the bottom diodes are replaced with comparator controlled NMOS transistors. While the comparator driven active rectifier is used in many designs, there are many methods to implement the comparator. By replacing the diodes with MOSFETs, the voltage drop across the bridge circuit is simply the drain-source voltage drop of the transistors. However, the active rectifier configuration results in the top two cross coupled NFETs always providing a path for reverse current when the AC signal is greater than the threshold voltage of the transistor. Thus, any delay in the comparator will result in reverse current and greatly degrade the power conversion efficiency of the circuit.
2 Implementation

2.1 Comparator delay compensation

The voltage conversion ratio and power conversion efficiency of active rectifiers are highly dependent on the performance and power consumption of the two comparators. Due to the delay of comparators, NMOS is not turned on and off at the exact time that AC input crosses DC output as would be expected in ideal case. This leads to two limitations to the efficiency of the rectifier. First, turning on NMOS later than the cross point reduces the effective period for charging output capacitance, which is detrimental to the voltage conversion ratio. Second, turning the NMOS off later causes the output capacitance to charge the input source, causing reverse current and harming the efficiency. This phenomenon is exacerbated at low input voltage because of the longer delay of comparators; therefore the minimum input amplitude is limited, which is bad for many applications.

2.2 Comparator design

A new comparator including a state machine to control the offset is introduced and shown in Fig. 3. Schematically, the input stage is a high gain differential amplifier (amplifies the difference between the inputs, but rejects the common mode component), followed by a decision making unit (latch), which ensures a sharp transition from one logic state to another. The high gain of the analog amplifier stage may be achieved using one or more stages. The latch is usually followed by a buffer stage to handle large capacitive loads.
latch stores the current state, which is set by the output of opposite comparator and is reset by the output of this comparator. Two additional paths are used to add bias in the comparator by injecting different currents into the paths of M5 and M6.

2.3 Novelty in proposed scheme

The newness in this proposed scheme is adding a fixed offset to the push-pull comparator, so that at both the turning on and turning off procedure of the comparator can have offsets that avoids the multi pulsing problem.

2.4 SR-Latch circuit

The basic function of the latch is to act as memory that keeps values for a whole clock period. It may also add some gain to the outputs. The latch provides an interface between analog and digital levels since the outputs of the comparator are digital. Otherwise if analog inputs are connected directly to the digital levels (the comparator outputs), the system becomes unstable. The digital levels can change quite much and can produce bounces even due to small noise spikes.

![Fig. 4. Schematic of SR-Latch circuit](image)

2.5 Bias generator

To set the reference current in the comparators, the comparator design needs a bias generator. Unlike a common reference generator, it is desirable to have smaller current at higher VDD so that the comparator can be faster at low VDD and save power at higher VDD. The schematic of the bias generator is shown in Fig. 5, which is a peaking current source. To achieve inversely proportional current, we needed to move the peaking to the lower voltage end of our design.

The aspect here is in between area and power. By using a resistor, smaller current can be achieved thus limiting of the comparator and improving the rectifier efficiency.

![Fig.5. Peaking current source](image)

3 Simulation and measurement results

3.1 Comparator output results

Analysis of the comparator switching times in Fig. 6 shows the comparator turning on before VAC > Vout thereby improving power efficiency of the rectifier and the output waveform for the high speed comparator is shown in Fig. 7.
In this proposed switched-offset scheme, delay time compensation is realized by comparators with time-varying offset voltages associated with specially designed current source, as shown in Fig. 5. The two comparators CMP1 and CMP2 are push-pull differential common-gate comparators, and the dynamic switched currents are also implemented in a push-pull fashion, for minimizing power consumption and also for reducing the comparator response time. When $V_{\text{Vin}^+} - V_{\text{Vin}^-} > |V_{\text{tp}}|$, $V_{\text{Vin}^+}$ is $V_{\text{AC}2}$ and $V_{\text{Vin}^-}$ is $V_{\text{AC}1}$ in Fig. 3) MP2 is turned on. When $V_{\text{Vin}^-}$ swings below 0 V, of CMP1 sinks a larger current than M2, causing M6 to source a larger current than M3 can sink, thus driving $V_{\text{out}}$ as well as $V_{\text{gn}1}$ high and turns on the active diode switch $M_{\text{N1}}$. As a result, the rectifier filtering capacitor $C_0$ is charged up by $V_{\text{Vin}}$. Note that in the previous phase, $V_{\text{gn}}$ has been high, causing $V_{\text{SW}}$ of CMP1 to be high, and the switches $M_{11}$ and $M_{12}$ are turned off. In the present phase, $V_{\text{gn}1}$ drives $V_{\text{SW}}$ low and turns $M_{11}$ on and $M_{12}$, allowing auxiliary bias currents from and to introduce the designed DC offset.
The sizes of the common-gate input pairs M1 through M4 are the same. The bodies of M1 through M4 are all connected to the on-chip ground, such that the threshold voltage of M1 and M4 would be smaller than threshold voltage of M2 and M3 when due to the body effect. The bias currents of M7 through M10 are 1X, 1X, 3X and 4X respectively. The current of M10 should be 3X (same as M9); however, taking body effect of M4 into consideration, it is set as 4X instead to make V2 even higher. The current ratio n is equal to four in our case, and the value of the dynamic artificial offset (around 100 mV) is set by the current ratios of M7 through M10. The auxiliary bias currents also serve as slew rate enhancement currents that charge up V1 and V2, starving M6 and feeding M1. Hence, Vout is pulled low, turning off the power switch MN1 right before Vin>0 prevent the occurrence of reverse current. A NOR SR-latch is added at each output of the comparators to avoid the aforementioned multiple-pulsing problem brought in by the dynamic offset scheme. Due to the NOR implementation of the SR-latch, VSW stays low even when Vgn1 goes low, such that M1 and M4 are saturated by the auxiliary bias currents, and prevent MN1 from turning on again in the same phase even if Vin- is still lower than 0 V, thus eliminating multiple pulsing.

To save static power, the power supplies of the comparators CMP1 and CMP2 are connected to (the distorted sinusoidal waveforms) Vin+ and Vin-, respectively, such that only one comparator is biased to work in every phase. This arrangement is good for the comparators to have more instant current and faster response.

4 Conclusions

In recent designs for biomedical implants, comparators driven active rectifiers being used. A robust switched-offset scheme for high-speed high-current active rectifiers is proposed and functionalities are demonstrated. Comparing the output of proposed active rectifier with conventional rectifier, much reduced ripple in proposed rectifier output and hence improvement in power conversion efficiency. The comparator turning on before Vin > Vout thereby improving power efficiency of the rectifier. The PEX extracted simulation shows some high frequency components in the comparator output while it is switching on or off. This is caused by a fast acting pole introduced due to parasitic capacitances.

In this research, for biomedical implants a switched-offset scheme for high-speed high-current active rectifier is proposed. Longer conduction time is achieved without sacrificing the robustness, and through careful design of the digital logic the multiple-pulsing problem related to dynamic offset is eliminated. A modified peak-current biasing circuit was implemented and measured in the proposed rectifier, verifying that it could operate efficiently over wide input amplitude and load current range. The comparators of the active rectifier are biased with novel QIPV biasing circuit, and reverse current is much reduced at low input voltage, and is eliminated at high input voltage. Compared to previous 13.56 MHz designs much
improved voltage conversion ratio and PCE at low input voltage and at heavy loading has been achieved. To conclude, to minimize the volume of biomedical implants by switching at high frequency; and to deliver an output power of tens of milli-Watt for neuron recorders and/or stimulators, the proposed rectifier operates at 13.56 MHz make it possible to use one secondary coil for both wireless power link and uplink data transmission.

References